REMARKS

Claims 1-26 are in the application of which claims 1, 12, 19, and 23 are in independent form. Claims 2-6, 13-17, 20, 21, 24, and 25 are indicated as containing allowable subject matter.

Claim objections

Claim 6 is amended to change the dependency from claim 1 to claim 2.

Claim 17 is amended to change the dependency from claim 12 to claim 13.

Rejections based on Ransijn

Claims 1, 7-11, 19, and 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Ransijn (US 6,347,128). For at least the following reason, the rejections should be withdrawn.

Independent claims 1, 12, 19, and 23 each recite: "wherein **the data signal has** embedded clock information and **a varying frequency**; ...." (Emphasis added.)

By contrast, in Ransijn, it is the **clock signal** (not the data signal) that has a varying frequency. For example, Ransijn, col. 1, lines 28-31, states: "Loop filter 14 low pass filters the phase detector output to provide a control voltage to VCO 16 to **adjust the clock frequency** (align the clock) so that it tracks the data rate of the data signal." (Emphasis added.)

Accordingly, the rejections should be withdrawn.

Rejections based on Iwamatsu

Claims 12, 18, 23, and 26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Iwamatsu et al. (US 5,867,542). For at least the following reason, the rejections should be withdrawn.

Independent claims 12 and 23 each recite: "wherein **the data signal has** embedded clock information and **a varying frequency**; ...." (Emphasis added.)

Iwamatsu does not describe varying the frequency of the data signal. Indeed, col. 11, lines 50 – col. 12, line 25 merely describe altering the phase of the **clock signal**. FIG. 2 of Iwamatsu does not show a data signal with varying frequency.

Note there are reasons for patentability in addition to those listed above.

Respectfully submitted,

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